Remarks:

At the time of the outstanding Office Action, the pending claims in the application were claims 40-52, 54-64, and 98-104. By this response, Applicant has (1) amended claims 40-52, 54-64, and 98-104, and (2) added new dependent claims 105-175. No new matter is present. The pending claims are now claims 40-52, 54-64, and 98-175. The independent ones of these claims are claims 40, 51, 52, 54, 100 and 102.

The outstanding Office Action identified claims 51 and 52 as being allowable if re-written into independent form. (See Office Action; page 8). Applicant has amended claims 51 and 52 into independent form by incorporating the limitations of antecedent claim 40. Applicant thanks the Examiner for his consideration of these claims and respectfully submits that these claims are in condition for allowance.

The outstanding Office Action also rejected the pending claims for alleged indefiniteness arising from the use of the pronoun "it". Applicant has removed this pronoun from independent claims 40, 51, 52, 54, 100 and 102. As such, Applicant respectfully submits that this indefiniteness rejection has been rendered moot and should be withdrawn.

The outstanding Office Action also rejected independent claims 40, 54, 100 and 102 for alleged anticipation based on the Dixon reference (USPN 4,464,718). Applicant respectfully disagrees with this rejection.

With reference to independent claim 40, Applicant first respectfully submits that Dixon fails to disclose the use of a "re-configurable logic device" as recited in claim 40. The patent application defines a "re-configurable logic device" as "any logic technology whose form and function can be significantly altered (i.e., reconfigured) in the field post-manufacture". (See Patent Application at paragraph 71 (with reference to this application's published version U.S. Pat. App. Pub. 2006/0294059) (emphasis added). The patent application further describes at paragraph 71 examples of re-configurable logic devices, including programmable logic devices (PLDs) (of which an FPGA is an example). By contrast, Dixon describes a system that offloads search tasks from a main processor using a "record scan circuit 20". Dixon's "record scan circuit" is not implemented with re-configurable logic. Instead, Dixon's "record scan circuit" is a hardwired combination of discrete logic elements (see Dixon; Figures 4-6). As such, neither the form nor the function of Dixon's "record scan circuit" can be significantly altered in the field post-manufacture. Given this failure, Dixon fails to anticipate claim 40.

Applicant also notes the independent claim 40 further recites the re-configurable logic device is "configured to receive and process streaming data through a pipeline deployed on the re-configurable logic device, the pipeline comprising a plurality of pipelined data processing engines, the plurality of processing engines being configured to perform different processing operations, wherein the pipeline comprises a multi-functional pipeline, and wherein the re-configurable logic device further comprises a control processor, wherein the control processor is configured to controllably activate or deactivate each processing engine in the pipeline and thereby define a function for the pipeline, the pipeline function being the combined functionality of each activated processing engine." An exemplary embodiment of this aspect of claim 40 is described in the patent application at paragraph 124 with reference to Figure 32 (see also Figures 29-30 and paragraphs 119-123).

> FIG. 32 depicts yet another exemplary pipeline wherein the pipeline 200 is comprised of multiple processing engines (each engine comprising one or more stages), each of which can be either activated by the control processor 204 such that the engine performs its recited task on the data it receives or deactivated by the control processor 204 such that is acts as a "pass through" for the data it receives. Activation/deactivation of the different engines will in turn depend on the functionality desired for the pipeline. For example, if it is desired to perform a search operation on encrypted and compressed data stored in the mass storage medium 26, the decryption engine 210, decompression engine 214, and search engine 218 can each be activated while the encryption engine 212 and compression engine 216 can each be deactivated. Similarly, if it is desired to store unencrypted data in the mass storage medium in a compressed and encrypted format, the compression engine 216 and the encryption engine 212 can be activated while the decryption engine 210, the decompression engine 214, and the search engine 218 are each deactivated. As would be understood by those of ordinary skill in the art upon reading the teachings herein, other activation/deactivation combinations can be used depending on the desired functionality for the pipeline 200. (Emphases Added)

Dixon fails to disclose the "multi-functional pipeline" deployed on a re-configurable logic device as recited in claim 40 where a "control processor" is configured to "controllably activate or deactivate each processing engine in the pipeline and thereby define a function for the pipeline". The only data processing operation deployed on Dixon's offload engine is the search operation performed by the "record scan circuit 20". As such, not only is Dixon's "record scan circuit" not a "multi-functional pipeline" that comprises "a plurality of pipelined data processing engines, the plurality of processing engines being configured to perform different

processing operations", but Dixon also fails to disclose that different processing engines in the pipeline can be controllably activated and deactivated to define the multi-functional pipeline's function.

Moreover, the Dixon reference fails to render claim 40 obvious as Dixon fails to teach or suggest to a person skilled in the art a multi-functional pipeline as recited in claim 40.

Therefore, for the foregoing reasons, Applicant respectfully submits that claim 40 is patentable over Dixon. Applicant further submits that independent claims 54, 100 and 102 are patentable over the Dixon reference for similar reasons. For example, independent claim 54 recites that the accelerator comprises "a reconfigurable logic device arranged such that data read from the hard disk drive streams through the reconfigurable logic device prior to being passed on to the processor, wherein the reconfigurable logic device is configured to process the data stream through a pipeline deployed thereon, the pipeline comprising a plurality of pipelined data processing engines, each processing engine being configured to perform a data processing operation on received data, and wherein the pipeline comprises a multi-functional pipeline, and wherein the reconfigurable logic device further comprises a control processor, wherein the control processor is configured to controllably activate or deactivate each processing engine in the pipeline and thereby define a function for the pipeline, the pipeline function being the combined functionality of each activated processing engine." Independent claim 100 recites that "the processing card comprises a re-configurable logic device, the re-configurable logic device comprising a multi-functional pipeline for processing streaming data received by the data processing card from the data source, the pipeline comprising a plurality of different pipelined data processing engines" and further recites "wherein each of the data processing engines is configured to be selectively activated and deactivated in response to control instructions to define a function for the-pipeline, the pipeline function being the combined functionality of the activated data processing engines." Lastly, independent claim 102 recites the following steps: "within a computer system comprising a processor and a reconfigurable logic device operating under control of the processor, streaming data through the reconfigurable logic device for processing thereby, the reconfigurable logic device comprising a multi-functional pipeline, the multi-functional pipeline comprising a control processor and a plurality of pipelined data processing engines, each processing engine being configured to perform a data processing operation on the data it receives", "the control processor selectively activating and deactivating the data processing engines in the pipeline to achieve a desired

pipeline function, the pipeline function being the combined functionality of the activated data processing engines", and "the activated data processing engines performing their data processing operations on the streaming data at hardware speeds."

Applicant further notes that the secondary reference, Wong (U.S. Pat. App. Pub. 2003/0163715), cited in the Office Action against various dependent claims of the patent application fails to bridge the gaps discussed above between the independent claims and Dixon. Wong describes a technique for securing the bit file used to configure an FPGA by encrypting that bit file. Before being loaded onto the FPGA to configure that FPGA, this encrypted bit file is decrypted (where this decryption may be performed by the FPGA itself (see Wong, paragraph 18)). Thus, Wong also fails to contemplate a multi-functional pipeline with multiple pipelined processing engines deployed in reconfigurable logic that are configured to perform different data processing operations, much less a design where the pipeline function can be changed by controllably activating/deactivating various processing engines in the pipeline to achieve a desired pipeline function. Instead, Wong's FPGA performs decryption.[1] If one wanted to change the function of Wong's FPGA, a person having ordinary skill in the art would understand that Wong requires a new "bit file" to be loaded onto the FPGA to reconfigure that FPGA for the new function. By contrast, with the invention of claim 40 a new configuration file does not need to be loaded onto the re-configurable logic device of claim 40 to change its function. Instead, one needs only to have the control processor controllably activate/deactivate different ones of the data processing engines and thereby change the pipeline's function. As such, claim 40 enhances throughput by avoiding a need to perform a relatively time intensive reconfiguration operation each time one wants to change the pipeline function. Applicant further submits that the other independent claims (claims 54, 100 and 102) are patentable over Dixon and Wong for similar reasons.

[1] At paragraph 23, Wong also hints that the FPGA may be configured to perform decompression ("portions of the data stream may be compressed and other portions of the data stream may be encrypted..."). However, it should be understood that even if this vague reference were interpreted as teaching the use of an FPGA to perform decryption and decompression, Wong clearly fails to teach the performance of such operations using pipelined data processing engines on the FPGA. Still further, Wong fails to disclose, teach or suggest that a control processor can be used to controllably activate/deactivate such decryption and decompression capabilities to achieve a desired overall function.

Conclusion:

For the foregoing reasons, Applicant respectfully submits that all pending claims are in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

Furthermore, Applicant believes that this amendment and remarks are sufficient for overcoming the rejections raised by this Office Action. However, should Applicant later need to further respond to these or new claim rejections, Applicant reserves the right to fully respond to these and any other new rejections, including but not limited to further amending the claims and/or adding new claims, submitting evidence in favor of the patentability of the claims, disputing the alleged prior art status of the cited references if warranted, and raising new arguments in favor of patentability. Moreover, in submitting this response, Applicant does not acquiesce to any characterizations of the claims or art (including any characterizations about what is allegedly known in the art) made in the outstanding Office Action.

A speedy and favorable action is respectfully requested.

Respectfully submitted,

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